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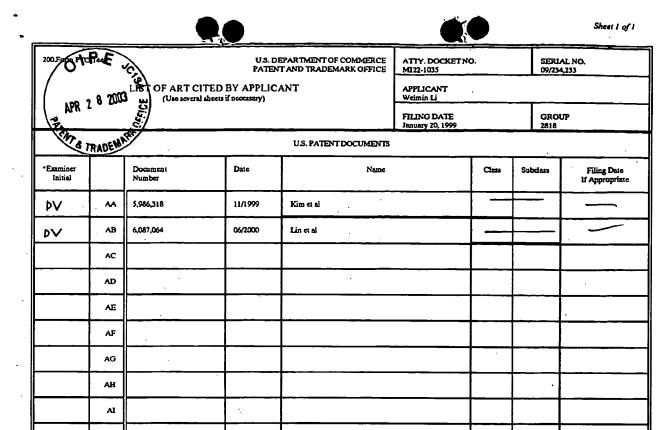
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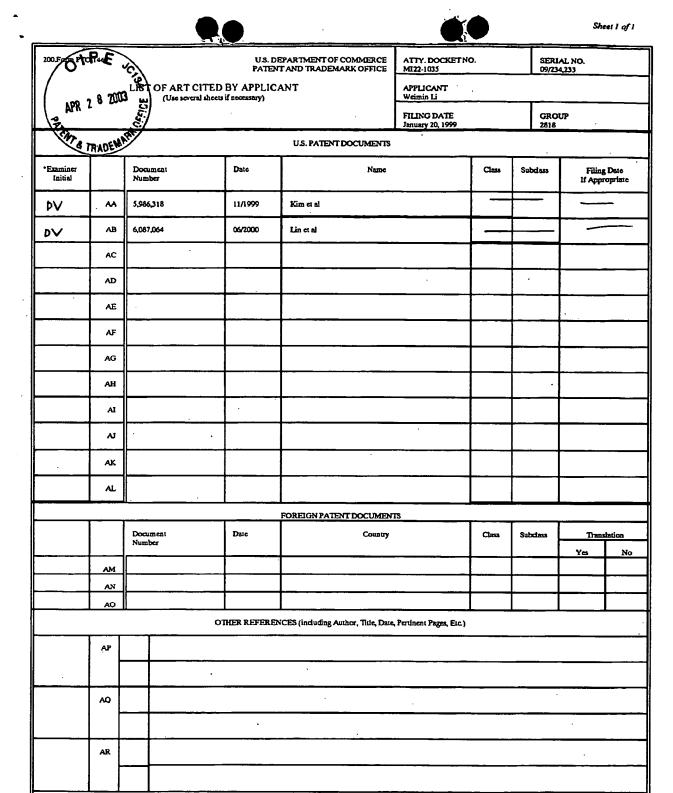
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		AL	4,695,859	9/1987	Guha et al		_				
	I	АМ	4,954.867	6/1990	Hosaka				h. n	· ·	
		AN	5,441,797	8/1995	Hogan					_	
	I	ΑO	5,710,067	1/1998	Foote						
	I	ΑР	5,759,755	6/1998	Park et al						
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(Use see al sheets if necessary) APPLICANT al sheets if necessary) FILING DATE January 20, 1999 GROUP 2818 **U.S. PATENT DOCUMENTS** *Examiner Document Date Name Class Subclass Filing Date Initial Number If Appropriate DV 5,670,297 09/23/97 Ogawa et al. AB 5,677,111 10/14/97 Ogawa AC 5,698,352 12/16/97 Ogawa et al. ΑD 5,831,321 11/03/98 Nagayama 01/07/97 ΑE 5,591,566 Ogawa ΑF 6,008,124 12/28/99 Sekiguchi et al. AG 5,340,621 08/23/94 Matsumoto et al. AH 5,600,165 02/04/97 Tsukamoto et al. ΑI 5,872,385 02/16/99 Taft et al. ΑJ 5,960,289 09/28/99 Tsui et al. AK 5,968,324 10/19/99 Cheung et al. AL 6,020,243 02/01/00 Wallace et al. FOREIGN PATENT DOCUMENTS Document Number Date Country Class Subclass Translation Yes No DV ΑM 0 588 087 A2 8/18/93 EPO DV AN 0 588 087 A3 8/18/93 EPO OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) ΑO A. Kiermasz et al.; "Planarisation for Sub-Micron Devices Utilising a New Chemistry"; Electrotech, February 1995; 2 pages DV ΑP IBM Technical Disclosure Bullatin *Low-Temperature Deposition of SiO2, Si3N4 or SiO2-Si3N4," Vol. 28, No. 9, p. 4170, Feb. 1986. DV ARTICLE: Bencher, C. et al., "Dielectric antireflective coatings for DUV lithography", Solid State Technology (March 1997), pp.109-AQ 114. DV grular id **EXAMINER** DATE CONSIDERED 10/11/01 *EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.

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	AC	5,800,877	09/01/98	Maeda et al.		_			
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	AK	5,968,611	10/19/99	Kaloyeros et al.	yeros et al.				
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	АМ	5,744,399	4/1998	Rostoker					
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	AD	6,12	24,641	9/26/00	Matsura			_			_	
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			Vol. 3049 (1997), pp	». 963-973.								
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